FIG.1

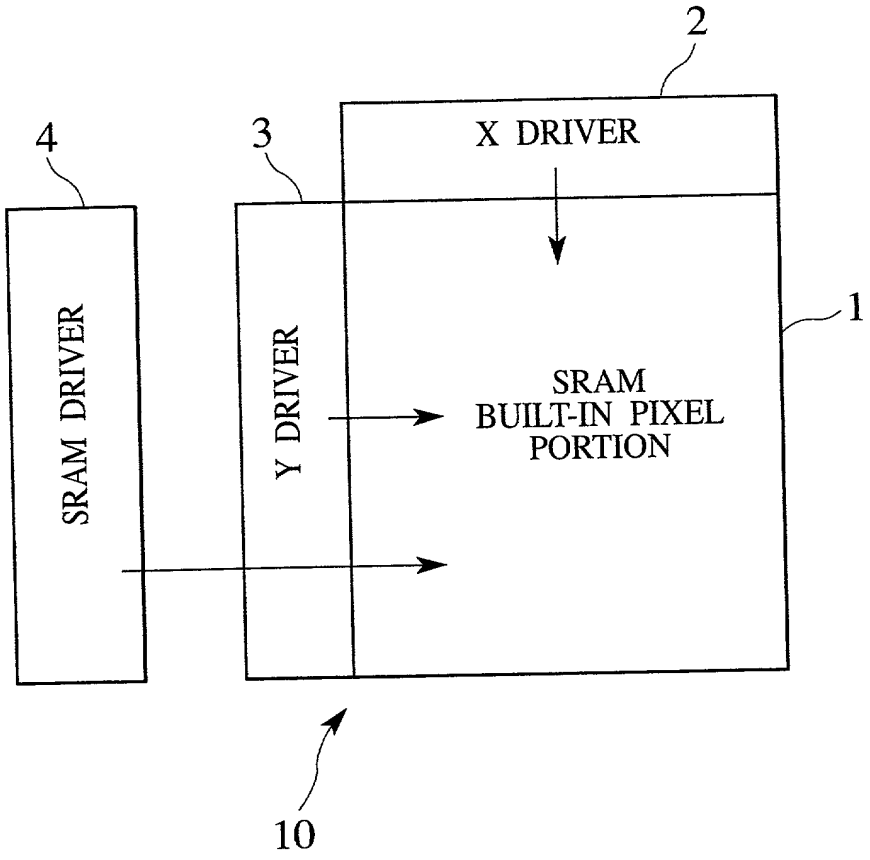

2
X DRIVER
4
3
SRAM DRIVER
Y DRIVER
1
SRAM
BUILT-IN PIXEL
PORTION
10

FIG.2

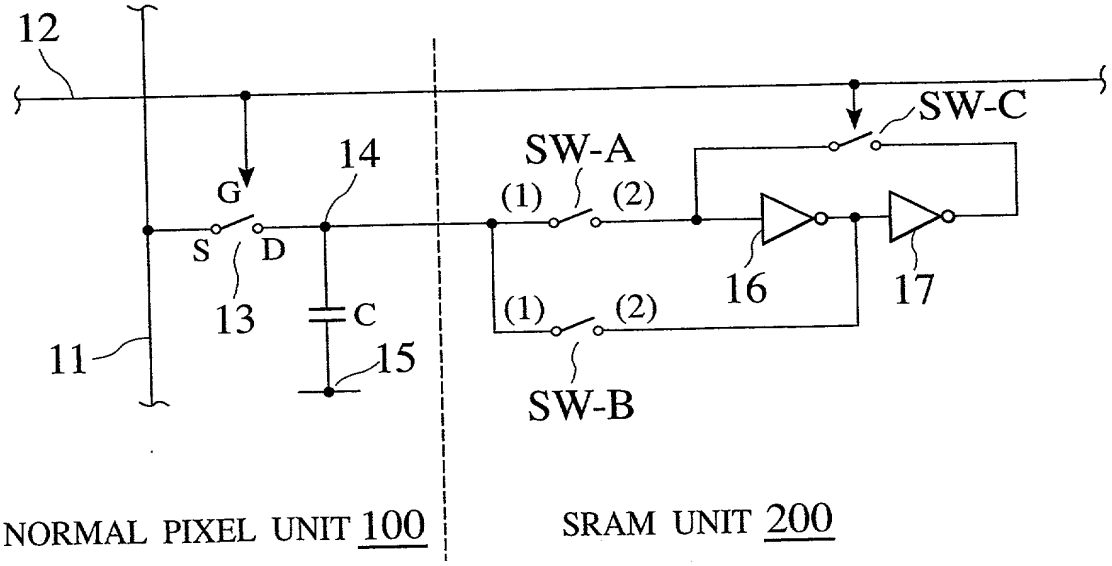
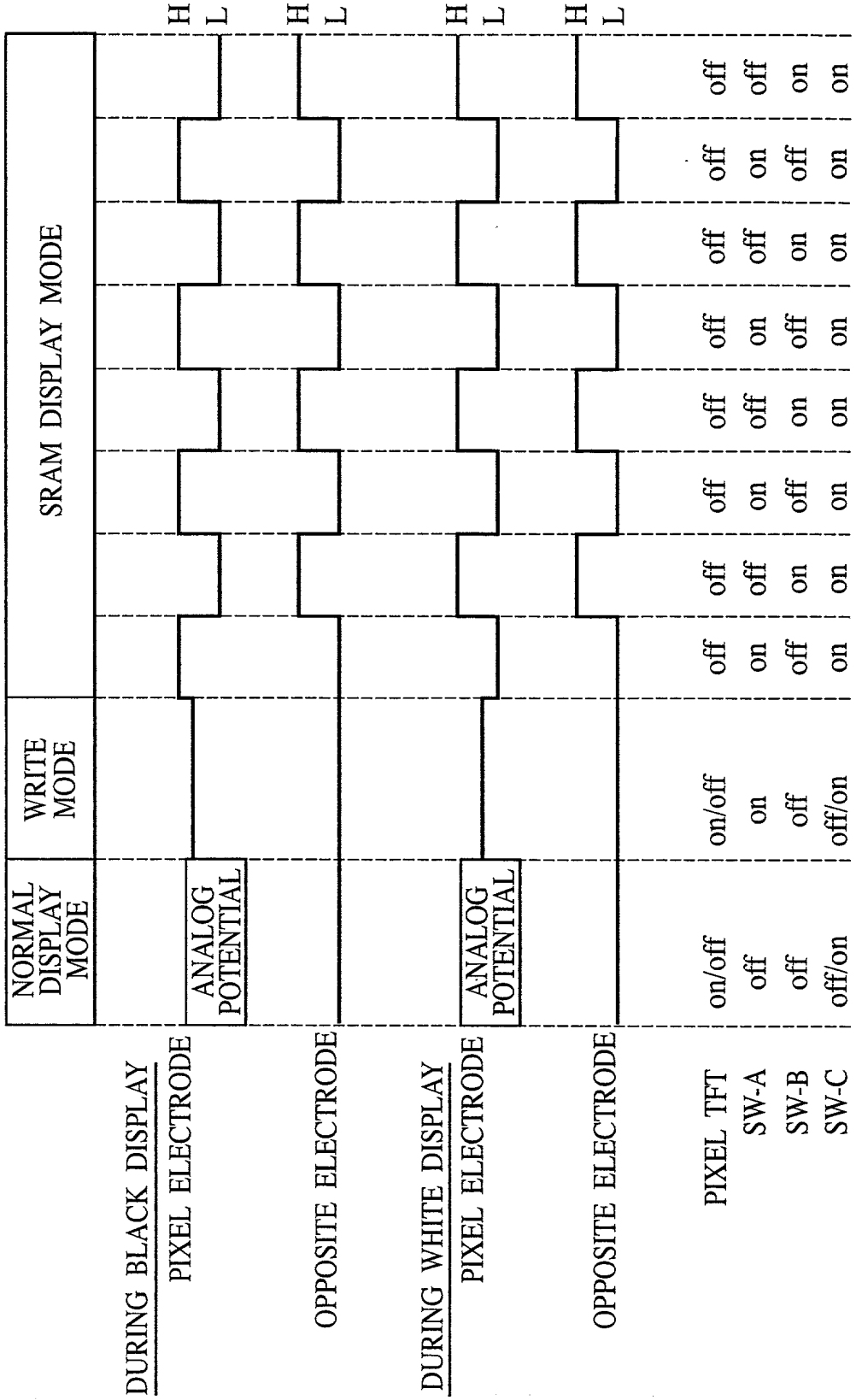

12
SW-C
14
SW-A
G
(1)
(2)
S
D
16
17
13
C
(1)
(2)
11
15
SW-B
NORMAL PIXEL UNIT 100
SRAM UNIT 200

FIG.3


NORMAL DISPLAY MODE
WRITE MODE
SRAM DISPLAY MODE
DURING BLACK DISPLAY
PIXEL ELECTRODE
ANALOG POTENTIAL
OPPOSITE ELECTRODE
DURING WHITE DISPLAY
PIXEL ELECTRODE
ANALOG POTENTIAL
OPPOSITE ELECTRODE
H
L
PIXEL TFT
SW-A
SW-B
SW-C
on/off
off
off
off/on
on/off
on
off
off/on
off off off on
on off on off
off on on off
on on on on
off off off off
on off on off
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off off off off
on off on off
off on on off
on on on on

FIG.4

CIRCUIT CONFIGURATION	POWER SOURCE VOLTAGE VDD	VSS	SRAM DRIVE
· X DRIVER SHIFT REGISTER DATA LATCH GRADATION VOLTAGE SELECTION UNIT SIGNAL LINE OUTPUT UNIT	XVDD	GND	UNREQUIRED
· Y DRIVER SHIFT REGISTER LEVEL SHIFTER SCAN LINE OUTPUT UNIT	YVDD YGVDD YGVDD	GND YGVSS YGVSS	REQUIRED REQUIRED REQUIRED
· SRAM DRIVER SRAM CONTROL SIGNAL GENERATING UNIT SRAM INVERTER POWER SOURCE UNIT	YGVDD SVDD	YGVSS SVSS	REQUIRED REQUIRED

FIG.5

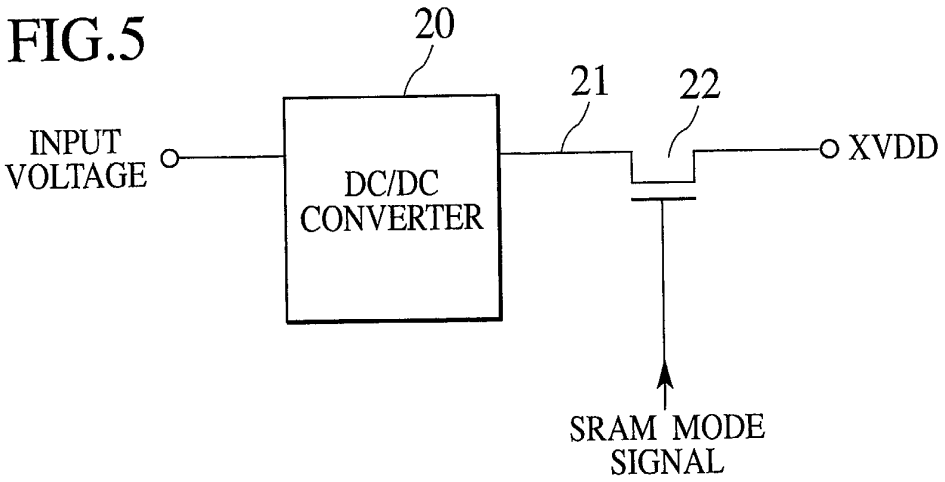

FIG.6